MSN12VD30-FR-VDC1
MSN12VD30-FR-VDA1
MSN12VD30-FR-VDT1

VR13 Digital Power Module

FEATURES:

- Maximum Load:30A
- Input Voltage Range from 4.5V to 16.0V
- Output voltage regulation range
  - 0.5V to 2.5V (10mV/step)
  - 0.25V to 1.52V (5mV/step)
- Compliant to Intel® VR13 DC-DC converter specifications
- Compliant to Intel® SVID protocol rev1.7
- Digitally programmable PID loop compensation
- Digitally programmable loadline slope and offset
- Digital temperature compensation
- PMBus™ rev 1.2 compliant serial interface
  - Query voltage, current, temperature faults
  - Fault Response
- Extensive fault detection and protection capability
  - IUVP, IOVP, OUVP, OOVP (fixed and tracking)
  - OCP instantaneous, averaged (total current), channel, and pulse-to-pulse current limit protection
  - Multiple internal and external OTP thresholds
  - Open/short voltage sense line detection
  - Negative current limit protection
- 14.2mmX7.8mmX6.35mm DFN Package

APPLICATIONS:

- Vcore power regulation for Intel® VR13 rev1.1 based Microprocessors
  - Servers, Workstations, and High-end desktops

GENERAL DESCRIPTION:

The MSN12VD30-FR series is a digital synchronous DC/DC power module provide power for Intel®VR13 applications. Command and monitor functions are controlled through the SVID interface which supports 5mV/step and 10mV/step VID tables, dynamic voltage identification (DVID), Power States (PS), and VR Data & Configuration Register requirements. The digital controller, power MOSFETs and most of support components are integrated in one hybrid package.

The module can support programmable temperature compensation to current sense allows the designer to tailor the response for best load-line accuracy over temperature. Best in class noise immunity is achieved through high over sample rate and digital current estimation. Protection features include a comprehensive suite of sophisticated over-voltage, under-voltage, over-temperature, and over-current protections. The module is a fully protected DC/DC solution that utilizes analog and digital functionality to maximize protection of the system.

The compact size enables utilization of space for highly density point of load to save the space and area. The thermal pad can enhance heat transferring capability. It is suitable for automated assembly by standard surface mount equipment and is Pb-free.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

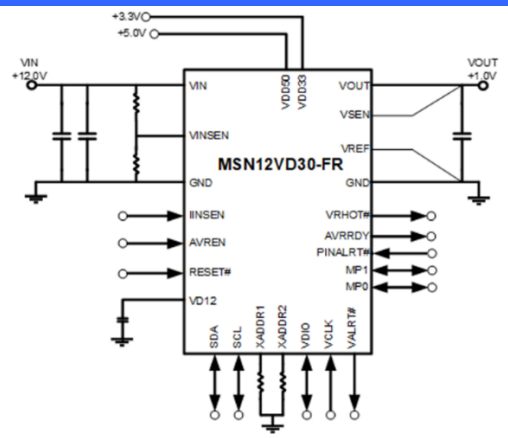


FIG.1 TYPICAL APPLICATION CIRCUIT

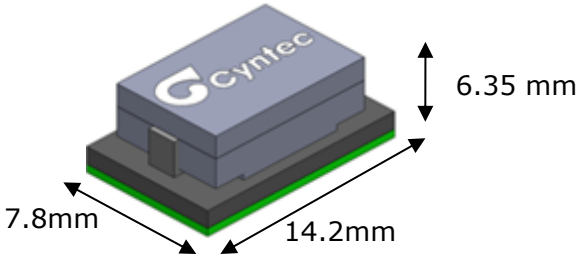


FIG.2 HIGH DENSITY POWER MODULE

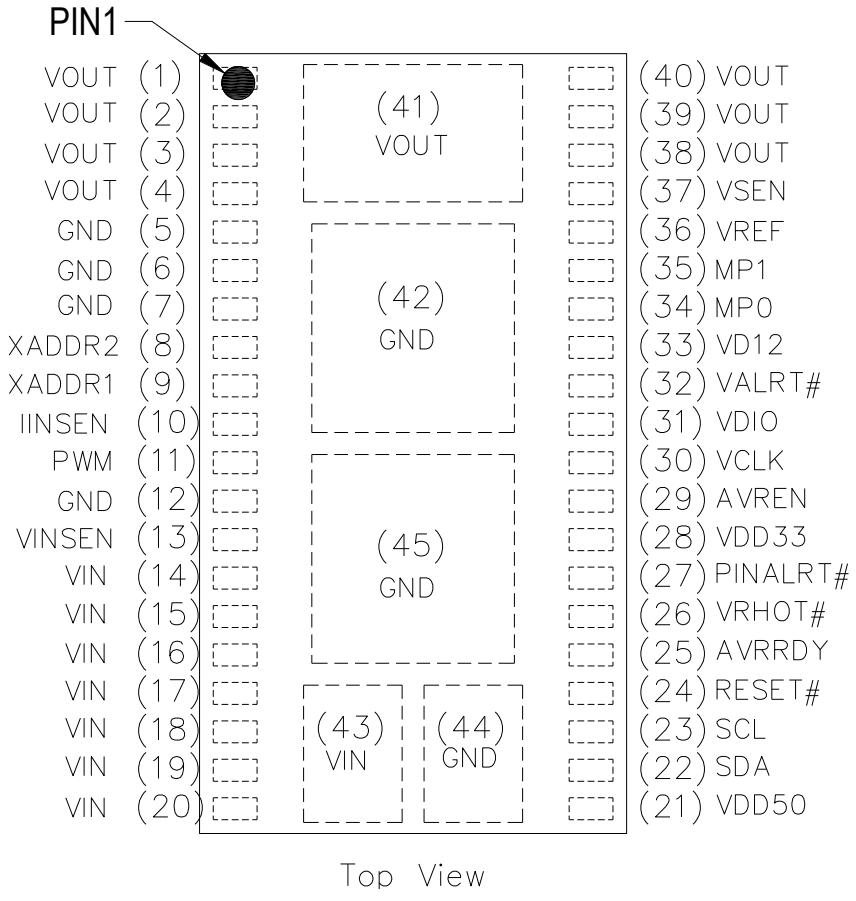
ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MSN12VD30-FR-VDC1 MSN12VD30-FR-VDA1 MSN12VD30-FR-VDT1	-40 ~ +85	DFN	Level 4	-

- This product is not recommended for second (back) side reflow.

Order Code	Packing	Quantity
MSN12VD30-FR-VDC1	Tray	540
MSN12VD30-FR-VDA1	Tray	540
MSN12VD30-FR-VDT1	Tray	540

PIN CONFIGURATION:



Top View

PIN DESCRIPTION:

Symbol	#	Type	Description
VOUT	1, 2, 3, 4, 38, 39, 40, 41	PWR	Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection. Place the output capacitors as closely as possible to this pin.
GND	5, 6, 7, 12, 42, 44, 45	PWR	Power ground pin. It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type and output capacitors as closely as possible to this pin.
XADDR2	8	Analog I	Used in conjunction with XADDR1, the I2C address of the module is set by tying an external resistor between this pin and GND.
XADDR1	9	Analog I	Used in conjunction with XADDR2, the I2C address of the module is set by tying an external resistor between this pin and GND.
IINSEN	10	Analog I	Current sense input used for PWR_IN calculation. An external amplifier or the PI sense network may be used to translate current information from a precision sense resistor to an input signal for the module. Refer to the Power Input Sense section herein for details. If unused, this pin may be grounded.
PWM	11	Analog O	Pulse Width Modulation (PWM) output. This signal is used to drive the PWM input of the power stage/FET driver IC. Unused PWM pins should be left unconnected (floating).
VINSEN	13	Analog I	VIN (+12V) voltage sense input. The VINSEN pin may be connected to the +12V supply through a resistor divider, or to the PI sense network and is used to guarantee a valid input voltage before starting up (input under-voltage lockout). Refer to the Power Input Sense section for details.
VIN	14, 15, 16, 17, 18, 19, 20, 43	PWR	Power input pin. It needs to connect input rail and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type capacitor as closely as possible to this pin.
VDD50	21	PWR	5.0V power supply input to the power MOSFETs. This pin should be connected to the system +5.0V supply and decoupled using high quality2.2μF ceramic capacitors.
SDA	22	Digital I/O	SMBus/I2C bi-directional serial data signal.
SCL	23	Digital I/O	SMBus/I2C bi-directional serial clock signal.

PIN DESCRIPTION:(Cont.)

Symbol	#	Type	Description
RESET#	24	Analog I	RESET# feature allows module to be put into lowest power dissipation mode. This pin may be left floating if unused but it is recommended that a 1kΩ pull up to 3.3V be used if this signal is connected to a trace on the board.
AVRRDY	25	Analog O	Voltage regulator "Ready" output signal. The AVRRDY indicator will be asserted when the module is ready to accept SVID commands after AVREN is asserted. This open-drain output requires an external pull-up resistor (1kΩ recommended). AVRRDY will be pulled low when a shutdown fault occurs.
VRHOT#	26	Analog O	Active low external temperature indicator. VRHOT# is asserted at the temperature defined by the programmable TEMP_MAX register.
PINALRT#	27	Analog I	Configurable as PVID voltage selection pin. Refer to table 2 default setting table to set the output voltage. If PINALRT#=1, it is recommended that a 1kΩ pull up to VDD33. If PINALRT#=0, it is recommended to pull down to ground.
VDD33	28	PWR	3.3V power supply input to the digital controller. This pin should be connected to the system +3.3V supply and decoupled using high quality 2.2μF ceramic capacitors.
AVREN	29	Analog I	Active high Output Enable input. Asserting the AVREN pin will activate the digital module, pending status of the internal power-on-reset circuit and any existing fault states. De-asserting then asserting AVREN after a latched-fault based shutdown will cause the module to enter the soft start state. Faults will be cleared when AVREN is reasserted.
VCLK	30	Digital I	SVID clock interface.
VDIO	31	Digital I/O	SVID bi-directional data interface.
VALRT#	32	Digital O	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed.
VD12	33	PWR	Do not apply voltage to or ground this pin. Internally generated 1.2V voltage reference used to power digital core logic. The pin is provided for attaching external decoupling capacitors only. Decouple using high quality 1.0μF + 0.1μF ceramic capacitors .This pin is not intended to be used to drive external components as +1.2V reference.
MP0	34	Digital I/O	Multi-purpose pin-0 configurable as PVID voltage selection pin. Refer to table 2 default setting table.
MP1	35	Digital I/O	Multi-purpose pin-1 configurable as PVID voltage selection pin. Refer to table 2 default setting table.
VREF	36	Analog I	Voltage sense inputs. VSEN (+) and VREF (-) are inputs to the precision differential remote sense amplifier and should be connected to the sense pins of the remote load.
VSEN	37		

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND	Note 1	-	-	+16.5	V
VDD50 to GND	Note 1	-0.3	-	+8.0	V
VDD33 to GND	Note 2	-0.3	-	+4.0	V
VCLK, VDIO, VALRT# to GND	Note 1	-0.3	-	+1.35	V
VSEN to GND	Note 1 (Do not exceed VDD33 + 0.2V)	-0.3	-	+3.7	V
VREF to GND	Note 1 (Do not exceed VDD33 + 0.2V)	-0.3	-	+0.5	V
VD12	Note 1 (Do not drive or load this pin)	-1	-	+1	mA
VOUT to GND	Note 1	-	-	+3.3	V
	All other pins (Note 1, Note2)	-0.3	-	+4.0	V
Tc	Case Temperature of Inductor	-	-	+110	˚C
Tstg	Storage Temperature	-40	-	+125	˚C
HBM	Human Body Model	-	-	2	KV
CDM	Charged device model	-	-	500	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+4.5	-	+16	V
VOUT	Adjusted Output Voltage	+0.5	-	+2.5	V
IOUT	Output Current	-	-	30	A
Ta	Ambient Temperature	-40	-	+85	˚C
■ Thermal Information					
Rth(j-a)	Thermal resistance from junction to ambient (Note 3)	-	11.5	-	°C/W

NOTES:
1 Parameters guaranteed by power IC vendor design and test prior to module assembly.
2 The absolute maximum VDD supply voltage is 4.0V with the conditions that the junction temperature range is maintained between -40°C ≤ TJ ≤ +125°C and the product is not operated at the absolute maximum VDD supply voltage for more than 24hours cumulatively over the lifetime of the module.
3 Rth(j-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 80mm×80mm×1.6mm 2 Oz with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards and VIN=12V VOUT=1.0

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 2Oz 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN=12V, VOUT=1.0V, Cin= 10uF/16V x3, 0.1uF/50V x1, Cout = 470uF/2V x 3 POSCAP, 22uF/6.3V ×7, 10uF/6.3V ×5.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
IQ(IN)	Input supply bias current	Vin= 12V, Iout=0A Vout =1.0V, AVREN=3.3V	-	21	-	mA
IS(IN)	Input supply current	Vin= 12V, AVREN = 3.3V Iout = 30A,Vout =1.0V, Frequency=700kHz	-	2.8	-	A
VDD33	Input supply current	Vin= 12V, IOUT=0A	-	15	-	mA
VDD50	Input supply current	Vin= 12V, IOUT=0A	-	21	-	mA
■ Output Characteristics						
I_{OUT}(DC)	Output continuous current range		0	-	30	A
VOUT(DC)	Output Voltage Accuracy	Vin=12V Vout=1.0V	-0.5	-	+0.5	$\%V_{set}$
ΔVOUT /ΔVOUT	Line regulation accuracy	Vin= 5.0V to 12V Vout= 1.0V, Iout=0A	-5	-	+5	mV
ΔVOUT /VOUT	Load regulation accuracy	Iout = 0A to 20A Vin = 12V, Vout = 1.0V	-5	-	+5	mV
EFF	Efficiency	VIN=12V VOUT=1.0V IOUT=15A	-	91.9	-	%
		VIN=12V VOUT=1.0V IOUT=30A	-	88.8	-	%
■ Oscillator And Switching Characteristics						
FOSC	Frequency range	Factory setting Note 4	664	714	764	kHz
AVREN VIH	AVREN Input high voltage (VIH)		0.8	-	-	V
AVREN VIL	AVREN Input low voltage (VIL)		-	-	0.5	V
AVRRDY VOL	AVRRDY Output low voltage(VOL)	Open drain output, ILOAD = +5 mA	-	-	0.4	V
AVRRDY OC-HiZ	Output current in Hi-Z state	Pin driven to +3.4V	-1	-	1	uA

ELECTRICAL SPECIFICATIONS :(Cont.)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 2Oz 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN=12V, VOUT=1.0V, Cin= 10uF/16V x3, 0.1uF/50V x1, Cout = 470uF/2V x 3 POSCAP, 22uF/6.3V ×7, 10uF/6.3V ×5.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Serial Communication PMBUS DC Characteristics						
SCL, SDA, VIH	SCL, SDA, Input High Voltage	Configured as 3.3V buffer	2.4	-	3.3	V
SCL, SDA, VIL	SCL, SDA, Input Low Voltage		-	-	0.8	V
SCL, SDA, IOL	SCL, SDA, Input current	SCL, SDA, pin driven to 3.4V	-1.5	-	+1.5	uA
SCL, SDA, VOL	SCL, SDA Output Low Voltage	open drain output ILOAD = +5 mA	-	-	0.4	V
SCL, SDA, SALRT. CPIN	SCL, SDA, SALRT. Pin Capacitance	SCL, SDA, SALRT. **Note 4**	-	4	-	pF
■ Serial Communication SVID DC Characteristics						
VIDO, VCLK VIL	VIDO,VCLK, Input low voltage (VIL)	CPU I/O Voltage (VTT) = 1V **Note 4**	-	-	0.45	V
VIDO, VCLK VIH	VIDO,VCLK, Input High Voltage		0.65	-	-	V
VIDO, VCLK VHYST	VIDO,VCLK, Hysteresis voltage		0.05	-	-	V
VDIO, VALRTVOH	VIDO,VALRT Output high voltage	CPU I/O Voltage (VTT) = 1V	-	VTT	-	V
VDIO, VALRT RON	VDIO, VALRT Output on resistance	Output in low state **Note 4**	4	-	13	Ω
VDIO, VALRT OIL	VDIO, VALRT Output leakage current	pin driven to 1.1V	-1	-	1	uA
VDIO, VALRT, VCLK CPIN	VDIO, VALRT, VCLK Pin Capacitance	VDIO, VALRT, VCLK **Note 4**	-	-	4	pF
VRHOT#, PINALRT# VOL	VRHOT#, PINALRT# Output low voltage (VOL)	ILOAD = +5 mA	-	-	0.4	V
VRHOT#, PINALRT# Hi-Z State	VRHOT#, PINALRT# Output current in Hi-Z state	pin driven to 3.4V	-1	-	1	uA
VRHOT#, PINALRT# RON	VRHOT#, PINALRT# Output on resistance	Output in low state; **Note 4**	4	-	13	Ω
■ Other						
VINSENINR	VINSEN Input resistance		-	>1	-	MΩ
VINSENIVR	VINSEN Input voltage range		-	0 to 0.24	-	V
IINSEN IVR	IINSEN Input voltage range		-	0 to 1.2	-	V
RESET# VIL	RESET# Input low voltage	**Note 4**	-	-	0.4	V
RESET# VIH	RESET# Input high voltage	**Note 4**	VDD33-0.7	-	-	V
VSEN IVR	VSEN Input voltage range		-	0 to 2.55	-	V
VREF IVR	VREF Input voltage range		-	-0.3 to 0.3	-	V

ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 2Oz 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN=12V, VOUT=1.0V, Cin= 10uF/16V x3, 0.1uF/50V x1, Cout = 470uF/2V x 3 POSCAP, 22uF/6.3V ×7, 10uF/6.3V ×5.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Fault Protection Characteristics						
OUVP	Output under Voltage threshold	Note 4	-	0.4	-	V
	OUVP threshold accuracy		-20	-	+20	mV
OOVP	Fixed OOVP threshold accuracy		-20	-	-20	mV
OTP	Thermal protection threshold		-	145	-	℃
	Internal OTP threshold accuracy		-	±10	-	℃

Note 4: Not subject to production test – verified by design and/or characterization.

TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=1.0V)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 80mm×80mm×1.6mm, 2Oz 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. VIN=12V, VOUT=1.0V, Cin= 10uF/16V x3, 0.1uF/50V x1, Cout = 470uF/2V x 3 POSCAP, 22uF/6.3V ×7, 10uF/6.3V ×5. Part number: MSN12VD30-FR-VDC1

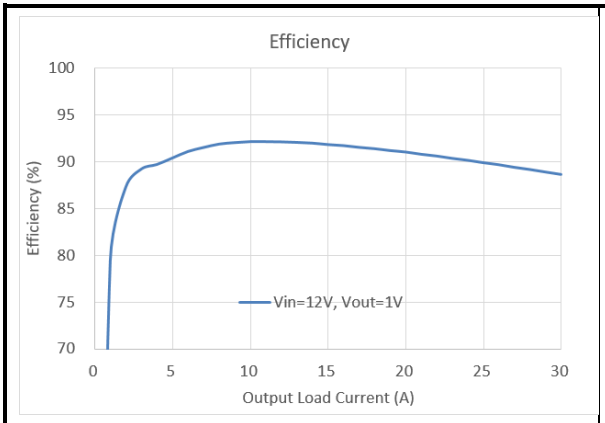


FIG.3 EFFICIENCY V.S. LOAD CURRENT (VIN=12V, VOUT=1.0V)

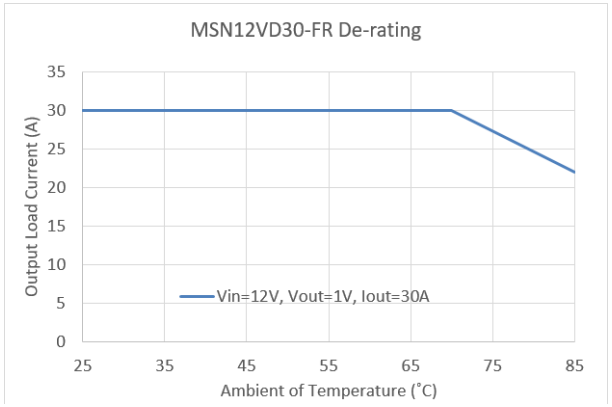


FIG.4 DE-RATING CURVE (VIN=12V, VOUT=1.0V)

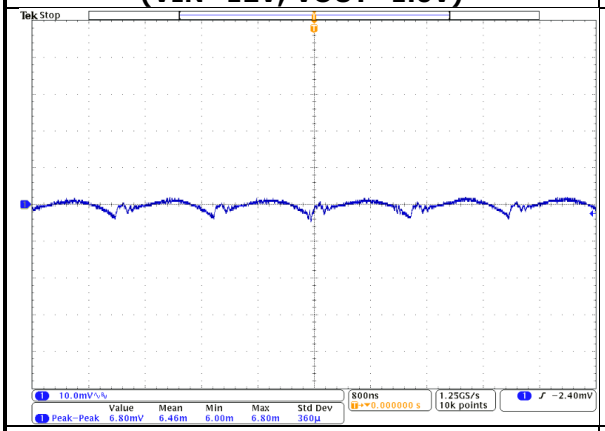


FIG.5 OUTPUT RIPPLE (12VIN, 1.0VOUT, IOUT=0A)

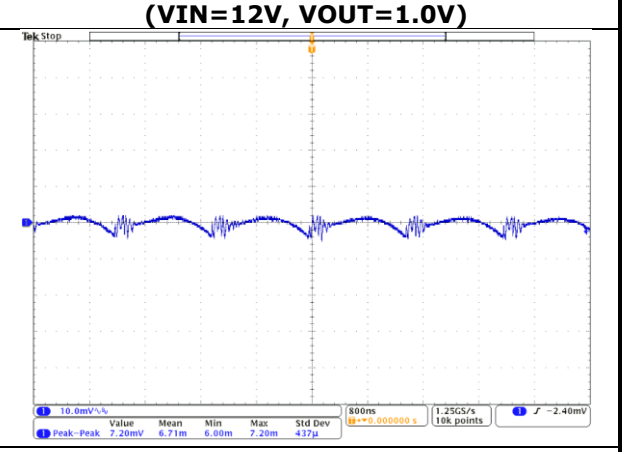


FIG.6 OUTPUT RIPPLE (12VIN, 1.0VOUT, IOUT=30A)

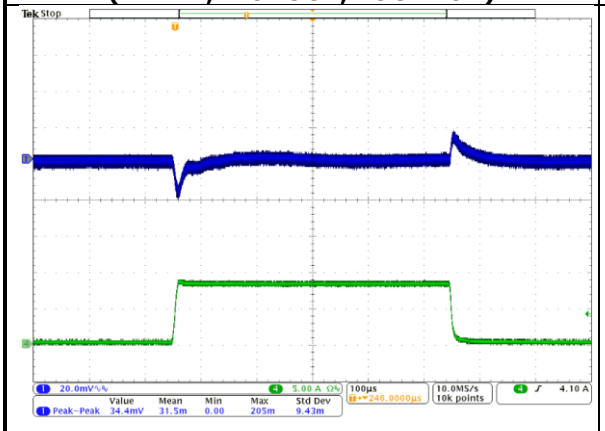


FIG.7 TRANSIENT RESPONSE (12VIN, 1.0VOUT, 0A to 8A LOAD STEP)

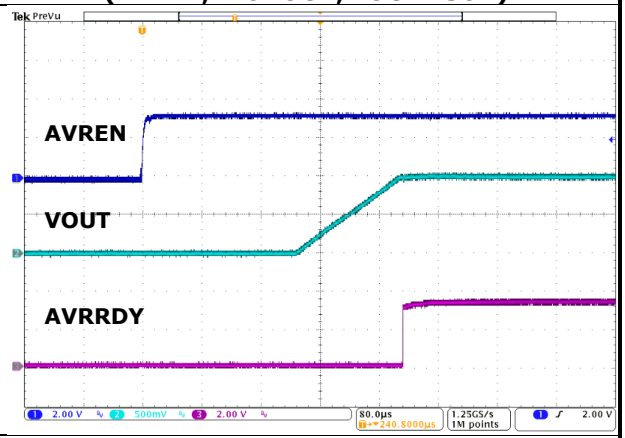


FIG.8 TURN-ON (12VIN, 1.0VOUT, IOUT=10A)

APPLICATION INFORMATION:

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

The FIGURE 9 shows the module schematics for input voltage +12V and output voltage +1.0 V.

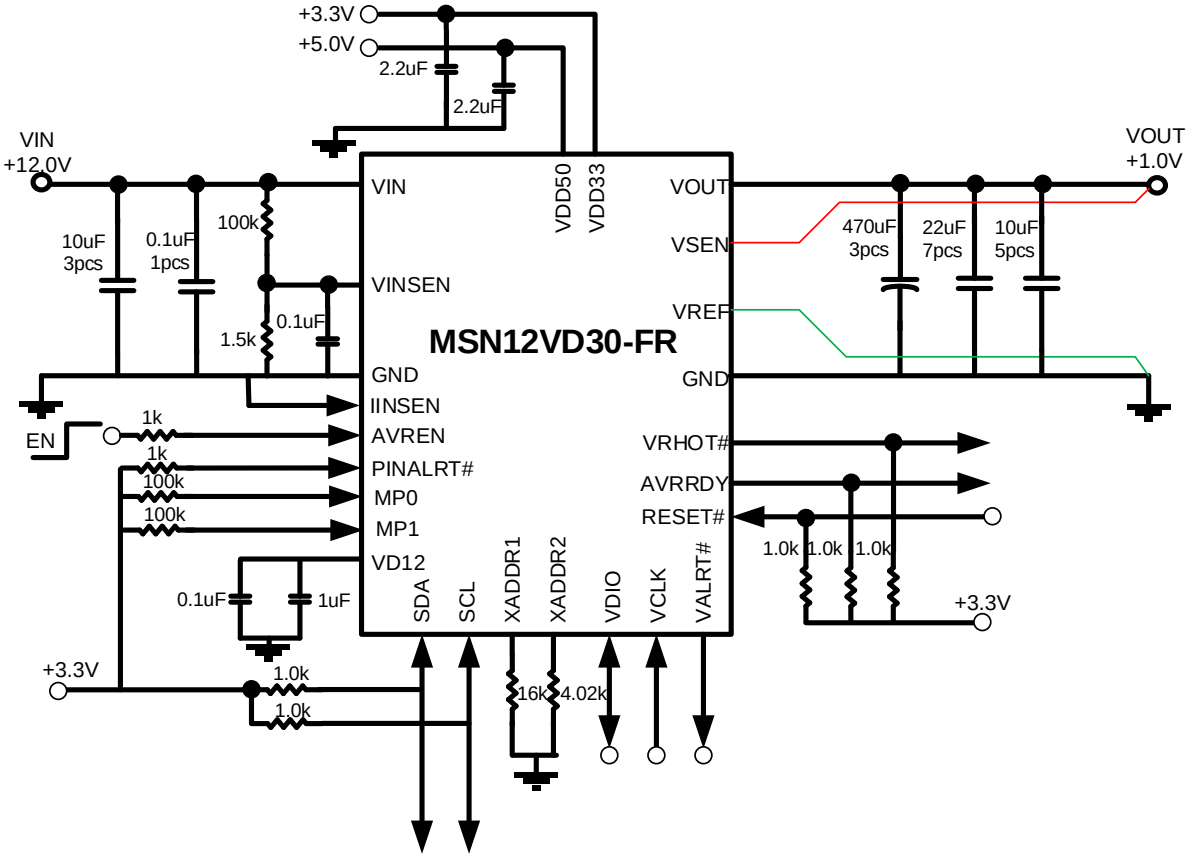


Figure.9 Typical application for power module operation

Maximum Output Capacitance Limitation:

MSN12VD30-FR series have different start up rate and make different maximum output capacitance limitation. If the output capacitance is over the maximum limitation, it is easy to trigger the INS_OCP at the soft start period. MSN12VD30-FR-VDC1 and MSN12VD30-FR-VDT1 start up rate are about 6.9mV/us and their output capacitor limitation are 2800uF without loading during start up. MSN12VD30-FR-VDA1 is about 16mV/us and its maximum output capacitor limitation is 1500uF without loading during start up.

STARTUP CONFIGURATION:

MSN12VD30-FR series are digital power module (Figure 10). Operation is controlled by application specific configuration settings loaded into control registers. For typical applications, the control registers are pre-programmed at the factory and stored in the on-chip nonvolatile memory (NVM). However, control registers can also be reprogrammed in the field via the serial communication (I2C) bus and stored into the NVM. MSN12VD30-FR series support up to 12 reprogramming cycles

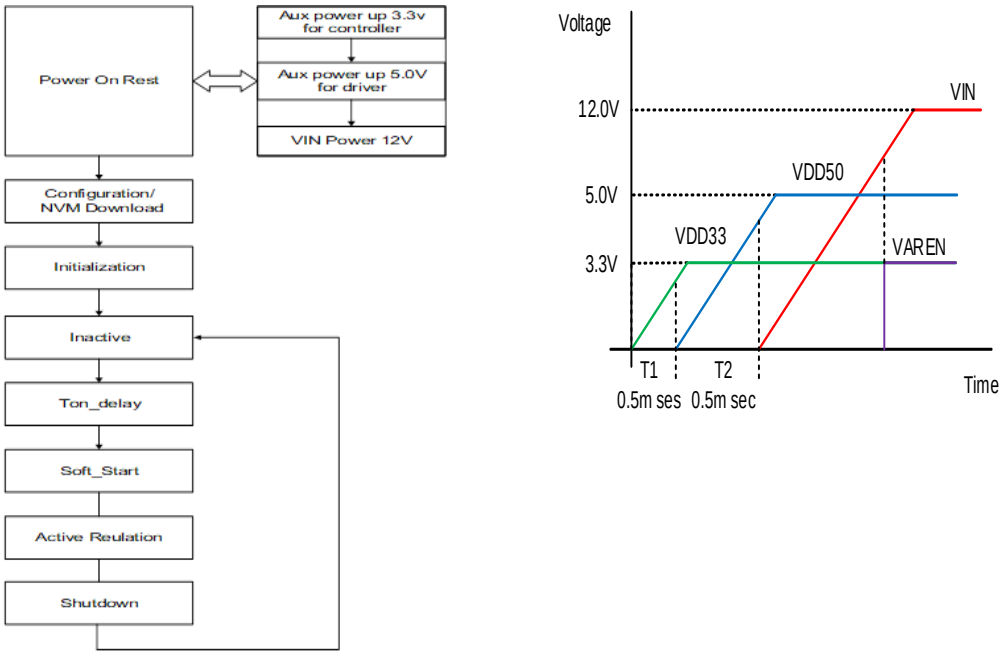


Figure 10 State machine

POWER-UP CONFIGURATION

Operating from a single +3.3V (VDD33) and +5.0V (VDD5.0) supply to the MSN12VD30-FR series, an on-chip low drop-out (LDO) regulator generates an internal +1.2V voltage. Module operation is initialized by an internal threshold based power-on reset circuit. During module configuration, the contents of the NVM are downloaded into the control registers. During this period, the PWM outputs are held in high impedance (Hi-Z) state, allowing board pull-up or pull-down resistors to set the correct default levels for static input signals such as the I2C address (XADDR1, XADDR2). The module provides a delay setting (config_delay programmable from 0ms to 51ms in 0.2ms increments) between power-on reset and entering the Initialization state. This delay is used to ensure the internal analog circuitry settles before making any precision measurements that are performed in the next state. If a strict power-on sequence synchronized by system AVREN is required, it is recommended that a minimum delay of 6ms be used from the startup of the VDD33 ramp up to AVREN assertion

INITIALIZATION

During the Initialization state, the module measures the internal and external temperatures, input voltage, and executes the various calibration routines within the MSN12VD30-FR series. Prior to exiting the Initialization state, the module performs the external resistor pin set measurements used to set the I2C and SVID serial addresses. To properly set the device addresses, resistors with 1% tolerance must be connected from the XADDR1 and XADDR2 pins to ground. Once a valid I2C address has been determined, communication with the module can established via the I2C bus of the module.

Resistor-to-GND (1%)		XADDR2							
		2.26k	**2.67k**	**3.16k**	**4.02k**	**5.36k**	**8.06k**	**16.0k**	**Open**
XADDR1	**2.26k**	FC	DC	BC	9C	7C	5C	3C	1C
	2.67k	F8	D8	B8	98	78	58	38	Reserved
	3.16k	F4	D4	B4	94	74	54	34	14
	4.02k	F0	D0	B0	90	70	50	30	10
	5.36k	EC	CC	AC	8C	6C	4C	2C	0C
	8.06k	E8	C8	A8	88	68	48	28	08
	16.0k	E4	C4	A4	84	64	44	24	04
	Open	E0	C0	A0	80	60	40	20	Reserved

Table 1: Device I2C Slave Address

POWER INPUT SENSE (VINSEN / IINSEN)

The digital power module provides the capability to estimate or measure the input power to the system. The input power supply is monitored for feed forward control, gain normalization, telemetry, power sequencing, maximum input power throttling, and fault detection.

The value of the input voltage used for calculation in both the input power estimation method and the external amplifier method can be configured as a fixed value entered by the designer, or as a measured value through a resistor divider as shown in Figure 9. If a resistor divider is used, the divided voltage is digitized through an internal ADC with an input referred range of 0 to 0.21V. A resistor divider network of R1 = 100kΩ and R2 = 1.50kΩ will allow the module to digitize a VIN range from 0V to 16.0V.

DIFFERENTIAL OUTPUT VOLTAGE SENSE (VSEN / VREF)

The remote differentially sensed output voltage of each loop (VSEN/VREF) is used for PID loop compensation, over voltage fault protection, and telemetry. The output voltage of all loops are sensed differentially and converted to a digital representation over a range of 0 to 3V using a high speed, precision analog-to-digital converter (ADC) with a resolution of 1.25mV.

VOLTAGE IDENTIFICATION (VID)

The digital module support the 8-bit VID tables as specified in the Intel VR13 and IMVP8 specifications for both ranges of 0.25V to 1.52V in 5mV steps and 0.5V to 2.5V in 10mV steps.

MP0/MP1

The MP0/MP1 is multi-purpose pin achieve difference output voltage when pin pull high or pull low. The default value is in table 2.

	MSN12VD30-FR-VDC1	MSN12VD30-FR-VDA1	MSN12VD30-FR-VDT1
PINALRT#=1, MP0=0, MP1=0	1.25V	0.72V	0.72V
PINALRT#=1, MP0=1, MP1=0	1.0V	0.75V	0.75V
PINALRT#=1, MP0=0, MP1=1	1.1V	0.85V	0.80V
PINALRT#=1, MP0=1, MP1=1	1.2V	0.95V	0.90V
Turn on Delay	0.2ms	0.2ms	2ms
VIN_ON	4.5V	4.5V	4.5V
Start-up rate	6.9mV/us	16mV/us	6.9mV/us
IUVP	4.25V / Latch	4.25V / Latch	4.25V / Latch
IOVP	15V / Latch	15V / Latch	15V / Latch
OUVP	0.4V / Hiccap	0.4V / Hiccap	0.4V / Hiccap
OOVP	1.4V / Hiccap	2V / Hiccap	1V / Hiccap
AVG_OCP	34A / Hiccap	34A / Hiccap	28A / Hiccap
INS_OCP	50A / Hiccap	50A / Hiccap	50A / Hiccap
OTP	145˚C / Latch	145˚C / Latch	145˚C / Latch
VRHOT# pin interrupt trigger	130˚C	130˚C	130˚C
Maximum Output Capacitor	2800uF	1500uF	2800uF

Table 2: Default setting table

DYNAMIC VOLTAGE IDENTIFICATION (DVID)

The digital module support Dynamic VID changes through the SVID commands SetVID_Fast, SetVID_Slow, and SetVID_Decay. The slew rate for the SetVID_Fast command is programmable in the range of 1 to 65 mV/us (a typical setting is 20 mV/us). The SetVID_Slow slew rate is programmable to either ¼ or ½ of the SetVID_Fast slew rate. When the SetVID_Decay command is received, the module allows the output voltage to decay at the rate determined by the load current and output capacitor bank. During dynamic VID changes, the tracking output over voltage protection (OOVP) is temporarily disabled. However, the fixed OOVP remains enabled.

INPUT POWER ON VOLTAGE (VIN_ON)

VIN must be greater than the VIN_ON threshold to start the system. If the enterprise controller has reached the Active Regulation state, it does not require VIN to remain above VIN_ON to maintain regulation. The default value is in table 2.

INPUT UNDER VOLTAGE PROTECTION (IUVP)

When the module is in Active Regulation state, VIN dropping below IUVP threshold will assert an IUVP fault which can be optionally programmed to shut down the system. If IUVP is not programmed as a shutdown fault, it can be used as a warning of VIN voltage sagging conditions. IUVP detection is enabled once VIN ramps above VIN_ON threshold after the Initialization state. VIN_ON and IUVP thresholds should be set above the FET driver UVLO threshold specification to ensure control of the power stages witching function. The default value is in table 2.

INPUT OVER VOLTAGE PROTECTION (IOVP)

When VIN is above the IOVP threshold, module can be programmed to shut down the system. With the recommended divider of 100kΩ and 1.50kΩ, the maximum IOVP threshold that can be set is 16.0V. The default value is in table 2.

OUTPUT UNDER VOLTAGE PROTECTION (OUVP)

An OUVP feature allows thresholds to be set relative to the target voltage. The programmable range is between 0mV to 500mV in 10mV steps. The default value is in table 2.

OUTPUT OVER VOLTAGE PROTECTION (OOVP)

This threshold is an absolute voltage with selectable values of 0.5V to 3V in 10mV increments. OOVP detection is always active after the Initialization state except during Open Sense Line fault detection. The default value is in table 2.

OVER-CURRENT PROTECTION (OCP)

The digital module calculates total current by summing the sampled phase currents from all active phases. The module provides two programmable OCP thresholds for total current:

- **Average Current OCP (AVG_OCP)**

  The digital module uses a low pass filter of programmable band width to determine the long term average total output current. The output of this filter is compared with the pre-programmed OCP thresholds for fault detection. Since this protection averages the output current over many switching cycles, the Average Current OCP threshold can be set very close to the expected maximum output load for accurate over current protection. It is recommended that the OCP threshold be set at number of active phases multiplied by the current handling capability of the power stage. The default value is in table 2.

- **Instantaneous Current OCP (INS_OCP)**

  The digital module can be programmed to provide an OCP fault protection based on 1, 2, 3, or 4 consecutive total current samples exceeding this threshold. Instantaneous Current OCP offers the fastest over-current protection, preventing possible output inductor saturation situations. Typically, this threshold is set higher than the Average Current OCP threshold to avoid nuisance tripping due to noisy current sense conditions. It is recommended that the instantaneous OCP threshold be set to 120% of the current handling capability of the power stage. The default value is in table 2.

When selected for shutdown, an OCP fault will trigger Hi-Z shutdown. OCP is enabled during the Soft Start, Active Regulation and closed-loop Shutdown states.

TEMPERATURE FAULTS PROTECTION

Over Temperature Protection (OTP) is provided by independently programmable shutdown thresholds for internal and external temperatures. Independently programmable alert thresholds are also provided for fault reporting purposes. All temperature related fault thresholds have a fixed 10 degree C hysteresis. When the detected temperature exceeds the programmed threshold, it must fall to at least 10 degree C below the programmed threshold before the fault is cleared. The default value is in table 2.

RESET MODE (RESET#)

The digital module can be configured to draw extremely low current (<1mA). When in Reset Mode, the module internal clocks are stopped which disables all functions. No communication to the device is possible. To enter Reset Mode, the RESET# pin must be grounded. Module will immediately go into a reset state. It is strongly recommended not to ground the RESET# pin during regulation as this may cause destructive behavior to the system. If the RESET# pin is pulled high, the module will wake up from reset and restart from power on reset state. The typical restart from reset may take up to 200ms.

VRHOT#

The VRHOT# fault is asserted when the external temperature exceeds the TEMP_MAX threshold as defined by the Intel VR13 PWM specification. VRHOT# is used for fault reporting only and cannot initiate a shutdown. VRHOT# has a fixed 3% hysteresis and is enabled after the Initialization state. The VRHOT# pin will be initialized in the Hi-Z state upon device power-up.

PINALRT#

The PINALRT# fault is asserted when input power exceeds the Pwr_in_alert threshold as defined by the Intel SVID protocol specification. PINALRT# is used for fault reporting only and cannot initiate a shutdown. PINALRT# will de-assert after 100ms and can be configured to report through the SMBus_Alert# signal.

SMBUS/I2C INTERFACE

All operating parameters in the digital module are configurable via the SMBus/I2C serial interface (SDA, SCL). The digital interface also allows for monitoring of fault status, as well as voltage, current, power, and temperature telemetry. The digital module support I2C bus speeds of 100 kHz and 400 kHz. The serial interface supports the following protocols as defined in the System Management Bus (SMBus) Specification (version 2.0, August 3, 2000).

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 11 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 6°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 150 seconds. Finally, keep at over 217°C for60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

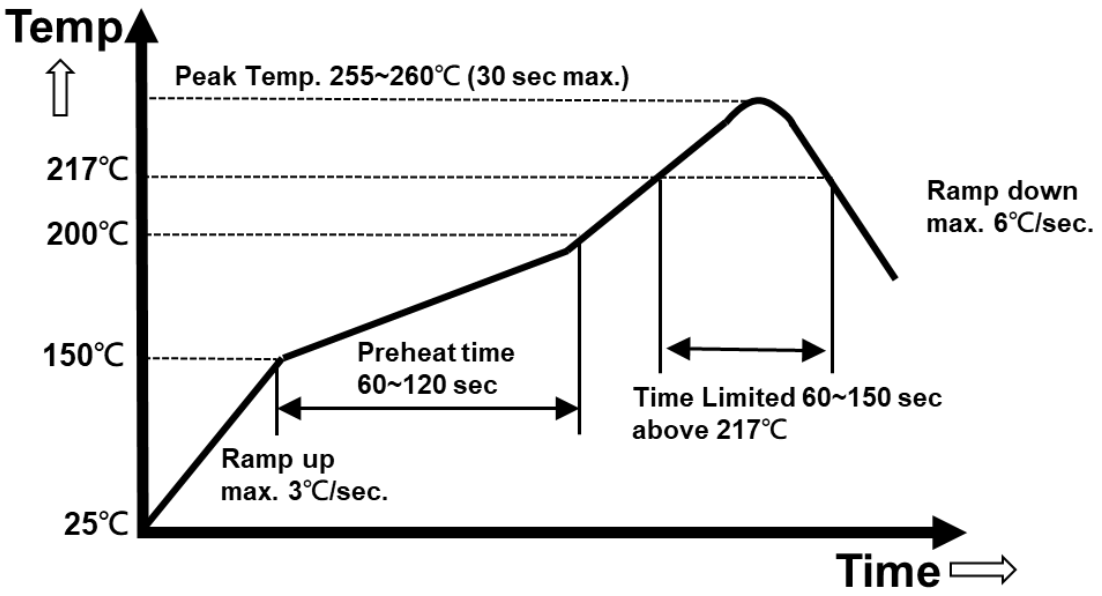


FIG.11 Recommendation Reflow Profile

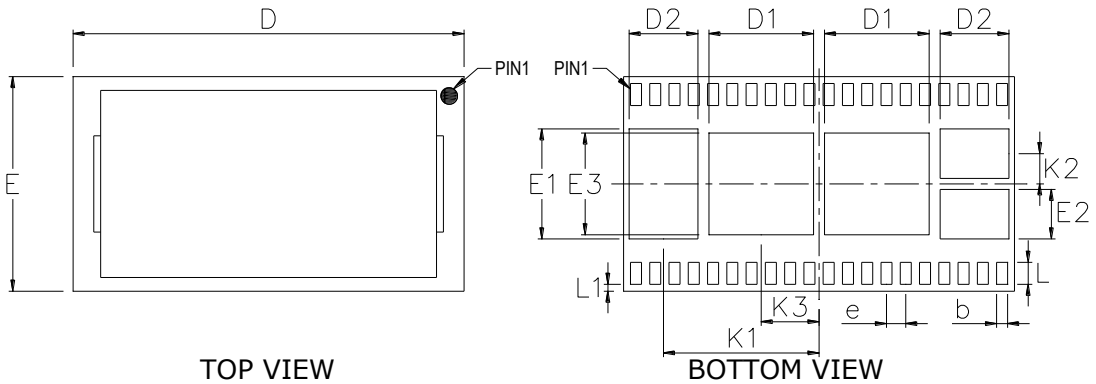
PMBUS PROTOCOL

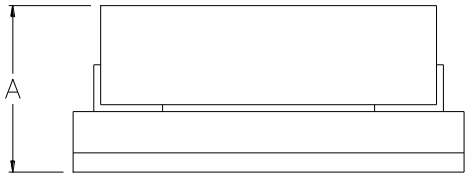
Command code	Command Name	Transaction Type	No. of bytes	Format	Range	Resolution	Units
0x00	PAGE	R/W Byte	1				
0x01	OPERATION	R/W Byte	1				
0x02	ON_OFF_CONFIG	R/W Byte	1				
0x03	CLEAR_FAULTS	Send Byte	1				
0x10	WRITE_PROTECT	R/W Byte	1				
0x15	STORE_USER_ALL	Send Byte	1				
0x16	RESTORE_USER_ALL	Send Byte	1				
0x19	CAPABILITY	Read Byte	1				
0x20	VOUT_MODE	R/W Byte	1				
0x21	VOUT_COMMAND	R/W Word	2	VID			
0x24	VOUT_MAX	R/W Word	2	VID			
0x25	VOUT_MARGIN_HIGH	R/W Word	2	VID			
0x26	VOUT_MARGIN_LOW	R/W Word	2	VID			
0x27	VOUT_TRANSITION_RATE	R/W Word	2	literal	0 : 50	1	mV/ms
0x28	VOUT_DROOP	R/W Word	2	literal	0 : 19.99	0.0098	mW
0x32	MAX_DUTY	R/W Word	2	literal	0 : 99.61	0.391	%
0x35	VIN_ON	R/W Word	2	literal	0 : 31.875	0.125	V
0x36	VIN_OFF	R/W Word	2	literal	0 : 31.875	0.125	V
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	2	literal	0 : 3.05	0.10	V
0x41	OUT_OV_FAULT_RESPONSE	R/W Byte	1				
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	2	literal	0 : 3.05	0.10	V
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	1				
0x46	OUT_OC_FAULT_LIMIT	R/W Word	2	literal	0 : 1023	1	A
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	1				
0x4F	OT_FAULT_LIMIT	R/W Word	2	literal	0 : 255	1	℃
0x50	OT_FAULT_RESPONSE	R/W Byte	1				
0x51	OT_WARN_LIMIT	R/W Word	2	literal	0 : 255	1	℃
0x55	VIN_OV_FAULT_LIMIT	R/W Word	2	literal	0 : 31.875	0.125	V
0x56	VIN_OV_FAULT_RESPONSE	R/W Word	1				
0x59	VIN_UV_FAULT_LIMIT	R/W Word	2	literal	0 : 31.875	0.125	V

PMBUS PROTOCOL

Command code	Command Name	Transaction Type	No. of bytes	Format	Range	Resolution	Units
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	1				
0x60	TON_DELAY	R/W Word	2	literal	0 : 51	0.2	msec
0x78	STATUS_BYTE	Read Byte	1				
0x79	STATUS_WORD	Read Word	1				
0x7A	STATUS_VOUT	Read Byte	1				
0x7B	STATUS_IOUT	Read Byte	1				
0x7C	STATUS_INPUT	Read Byte	1				
0x7D	STATUS_TEMPERATURE	Read Byte	1				
0x7E	STATUS_CML	Read Byte	1				
0x80	STATUS_MFR_SPECIFIC	Read Byte	1				
0x88	READ_VIN	R/W Word	2	literal			V
0x89	READ_IIN	R/W Word	2	literal			A
0x8B	READ_VOUT	R/W Word	2	VID			
0x8C	READ_IOUT	R/W Word	2	literal			A
0x8D	READ_TEMPERATURE_1	R/W Word	2	literal			˚C
0x8E	READ_TEMPERATURE_2	R/W Word	2	literal			˚C
0x94	READ_DUTY_CYCLE	R/W Word	2	literal			%
0x96	READ_POUT	R/W Word	2	literal			W
0x97	READ_PIN	R/W Word	2	literal			W
0x98	PMBUS_VERSION	Read Byte	1				
0x99	MFR_ID	R/W Word	2				
0x9A	MFR_MODEL	R/W Block	5				
0x9B	MFR_REVISION	R/W Block	1				
0x9C	MFR_LOCATION	R/W Block	1				
0x9D	MFR_DATE	Read Block	4				
0xD0	MFR_SPECIFIC_00	Read Block	2				
0xD1	MFR_SPECIFIC_01	R/W Block	2				
0xD3	MFR_SPECIFIC_03	Read Block	4				
Note: Literal = 11-bit mantissa (signed binary integer), 5-bit exponent (signed binary integer)							

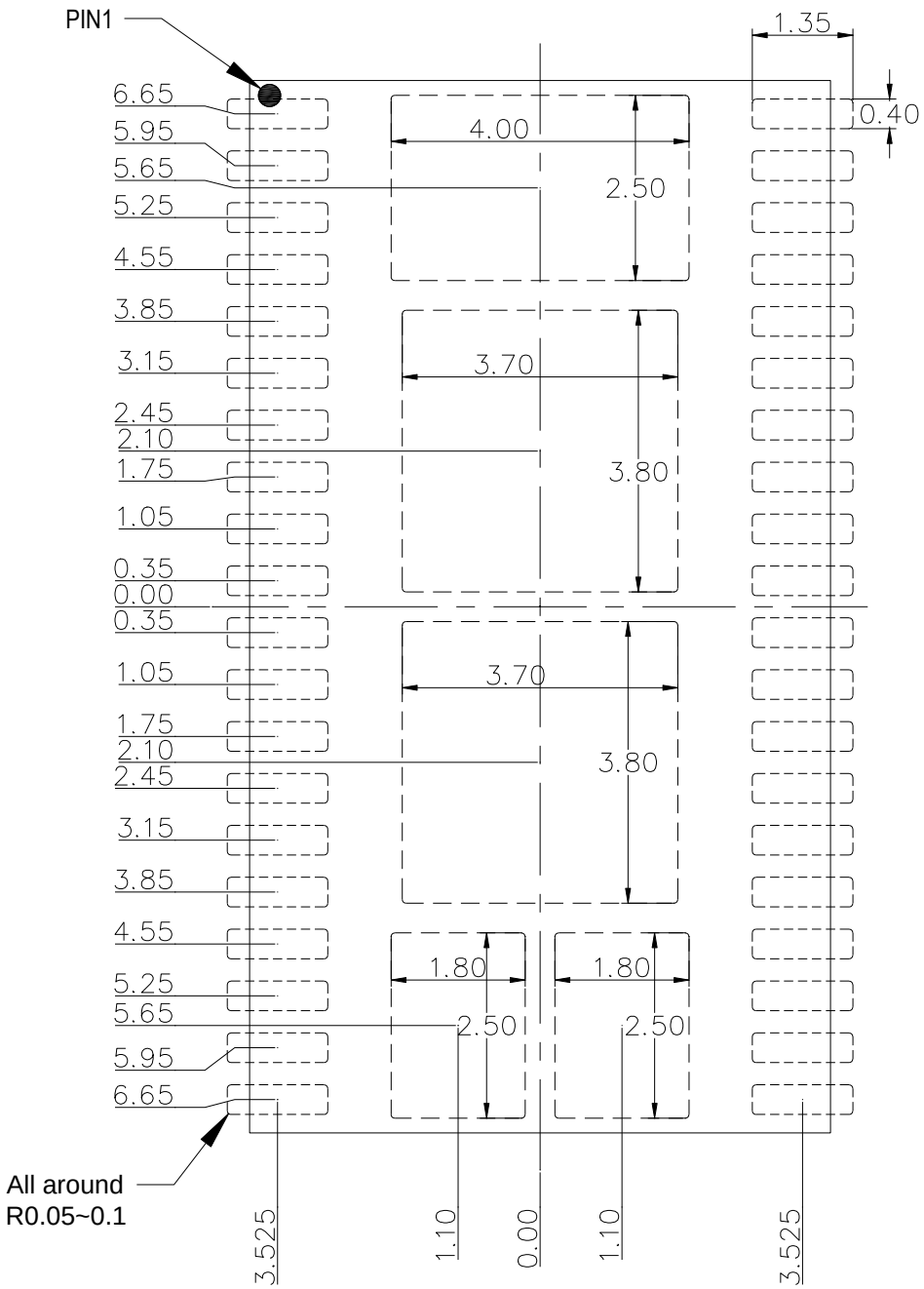
PACKAGE OUTLINE DRAWING:





DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	6.10	6.35
D	14.1	14.2	14.3
D1	3.70	3.80	3.90
D2	2.60	2.75	2.90
E	7.70	7.80	7.90
E1	3.90	4.00	4.10
E2	1.70	1.80	1.90
E3	3.60	3.70	3.80
K1	5.50	5.65	5.80
K2	0.95	1.10	1.25
K3	1.95	2.10	2.25
e	0.55	0.70	0.85
b	0.30	0.40	0.50
L	0.70	0.80	0.90
L1	0.10	0.25	0.40

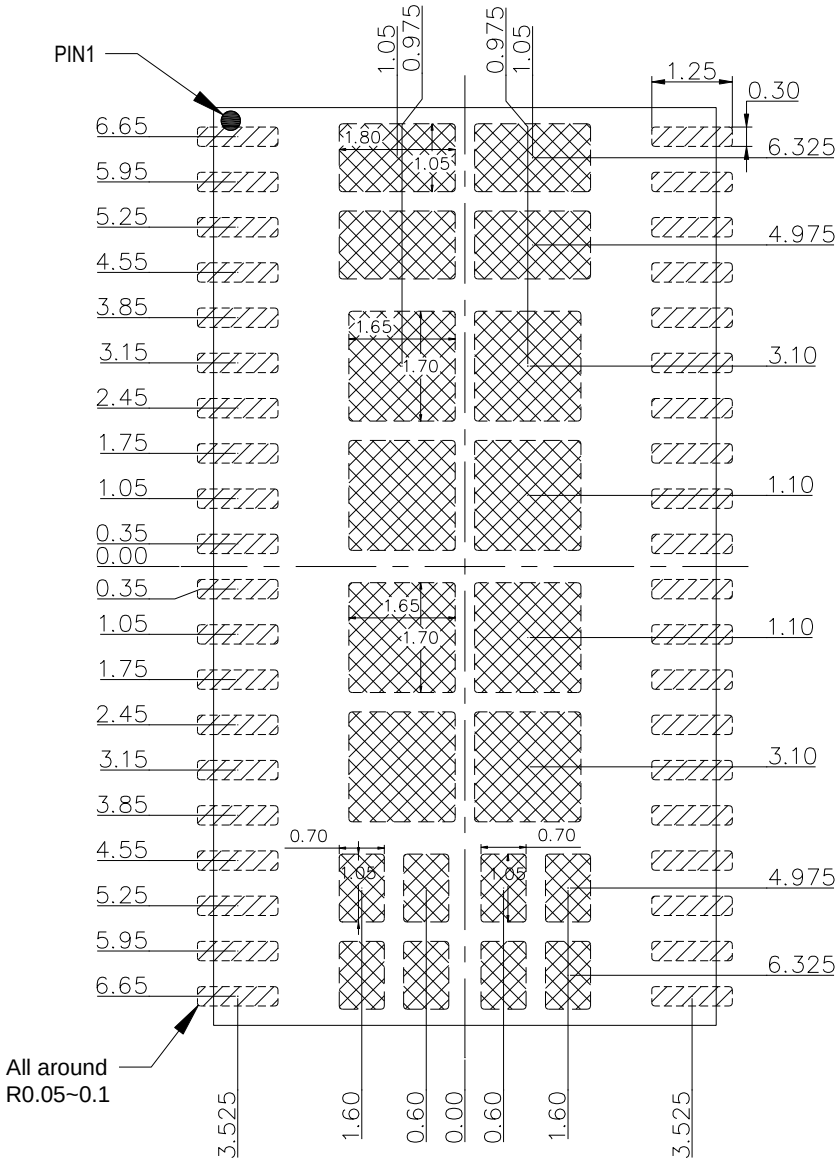
LAND PATTERN REFERENCE:



TOP VIEW

TYPICAL RECOMMENDED LAND PATTERN

LAND PATTERN REFERENCE:



Recommend 70%~100% land pattern area.

Recommend 50%~80% land pattern area.

TOP VIEW

STENCIL PATTERN WITH SQUARE PADS

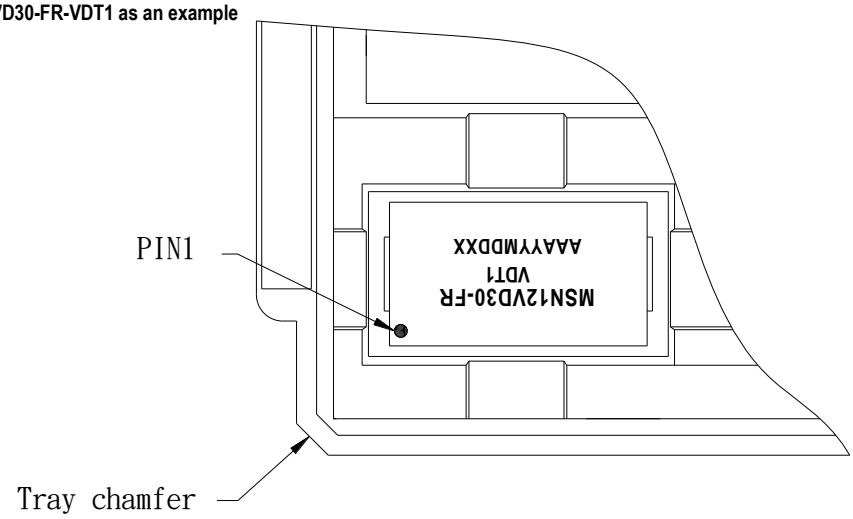
*Based on 0.1~0.15mm thickness stencil (Reference only)

PACKING INFORMATION:

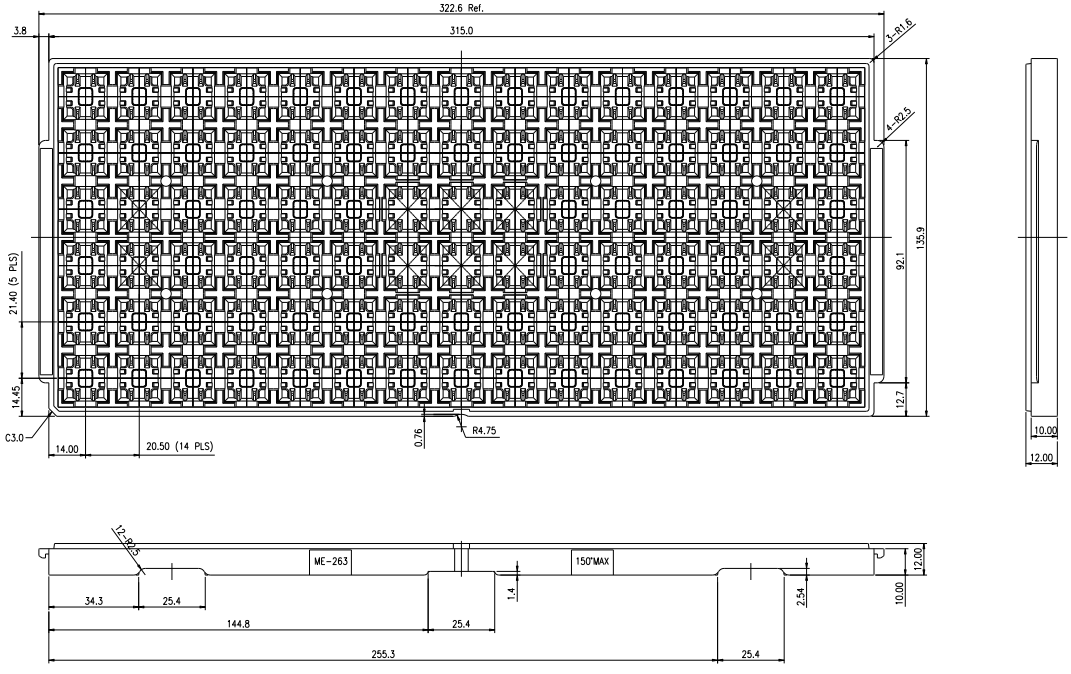
Unit: mm

Tray Packing

Take MSN12VD30-FR-VDT1 as an example



PACKAGE IN TRAY LOADING ORIENTATION



TRAY DIMENSION

REVISION HISTORY:

Date	Revision	Changes
2018.06.04	P01	Release the preliminary specification.
2018.07.26		Updated the pin define and land pattern reference.
2019.07.09	P02	Updated stencil pattern with square pads to stencil pattern with pads.
2019.12.06	P03	Updated power-up sequence information
2020.03.11	P04	Updated power-up sequence information Updated MP1 and MP0 output voltage function 1.0V change to 0.95V
2020.05.02	P05	MSL3 down to MSL4
2020.05.29	P06	Updated stencil pattern with square pads to stencil pattern with pads.
2020.07.16	P07	Updated packing information
2021.01.11	P08	Updated VIN Voltage for 14V to 16V
2021.11.10	P09	Modify the part number
2021.11.22	P10	Updated default setting table
2021.11.29	P11	Updated default setting table
2021.12.15	P12	Reference circuit for general application
2022.03.15	P13	Modify MSN12VD30-FR-VDC1, MP0=0, MP1=0, output voltage
2022.07.20	P14	Rth(j-a) and OUVP type error, Reflow parameter, land pattern reference
2022.08.19	P15	Modify MSN12VD30-FR-VDT1 AVG_OCP from 40A to 28A. Modify the typical performance characteristics turn on figure. Add the start-up rate to the default setting table.
2022.10.20	P16	Modify PINALRT# pin description. Add the maximum output capacitance limitation description and default setting table in the application information